REMARKS

This amendment is a full and timely response to the Final Office Action dated March 1, 2011. Claims 1-6 are pending, with claims 1, 3, and 5 being independent.

In this amendment, claims 1, 3, and 6 have been amended. Support for these amendments is variously found in the Applicant's specification as filed, including but not necessarily limited to the paragraphs ¶¶ [0042]-[0045] of the specification, as represented in U.S. Pub. No. 2006/0152461 A1. Reconsideration and allowance is requested in view of the following remarks. *No new matter has been added by these amendments.*

Claims 1-6 have been rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over *Edwards*, U.S. Patent Number 6,498,438 (*Edwards*). This rejection is respectfully traversed.

Independent claim 1, as amended, recites "[*a*] *method for operating a constant current circuit, comprising: after connecting a sampling capacitor connected between a gate and a source of a first transistor and a drain of the first transistor to a reference current source and setting a voltage across the sampling capacitor to a voltage between the gate and the source produced while the first transistor is driven by a reference current of the reference current source, cutting off the connection among the sampling capacitor, the first transistor and the reference current source, as well as connecting the drain of the first transistor to a buffer circuit, and driving the buffer circuit by a current of the first transistor due to the voltage between the gate and the source that is set in the sampling capacitor, wherein said cutting off the connection comprises applying a first signal to a gate of a second transistor connected between the drain of the first transistor and the reference current source, a second signal that is a logical inverse of said first signal to a gate of a third transistor connected between the gate and drain of the first transistor, a third signal to a gate of a fourth transistor connected between the drain of the first transistor and the buffer circuit, said setting the voltage across the sampling capacitor and said cutting off the connection occur within a precharge period to cause the constant current circuit to be temporarily connected to a source of a buffer circuit transistor of the buffer circuit during the precharge period, and the buffer circuit includes an analog buffer circuit and a precharge circuit; and executing a precharge processing for*

the precharge period by disconnecting the precharge circuit for the precharge period from the analog buffer circuit."

Edwards fails to disclose or suggest these claimed features. Specifically, Edwards fails to disclose "*cutting off the connection among the sampling capacitor, the first transistor and the reference current source, as well as connecting the drain of the first transistor to a buffer circuit, and driving the buffer circuit by a current of the first transistor due to the voltage between the gate and the source that is set in the sampling capacitor.*"

Consistently with this feature, the Office Action admits that *Edwards* does not disclose "a buffer circuit for driving the signal lines by a source follower circuit formed by connecting a constant current circuit; the buffer circuit drives the signal lines by a source follower circuit formed by connecting a constant current circuit to a source of a transistor." (Office Action Page 5).

Further, *Edwards*'s disclosure of a circuit 40 for producing an output current (at output 50) from an input word using switching transistors, and managing this output current via a transistor 70 in FIG. 6 (or T1 in FIG. 8) for resetting the voltage and a four transistor arrangement (T2 – T5) for avoiding a large voltage ramp at output 50. (*Edwards*, FIGs. 4-5c and 7d-8) does not disclose **Applicant's** "*wherein the buffer circuit includes an analog buffer circuit and a precharge circuit,*" or "*executing a precharge processing for the precharge period by disconnecting the precharge circuit for the precharge period from the analog buffer circuit.*"

In addition, the Office Action admits that *Edwards* does not discloses "*wherein said cutting off the connection comprises applying a first signal to a gate of a second transistor connected between the drain of the first transistor and the reference current source, a second signal that is* ***a logical inverse*** *of said first signal to a gate of a third transistor connected between the gate and drain of the first transistor.*" (Office Action Page 4).

Thus, *Edwards* does not disclose nor in any way suggest the Applicant's claimed features of independent claim 1.

Yamazaki does not remedy the deficiencies of *Edwards*.

Yamazaki is relied upon for purported disclosure of a digital to analog conversion circuit, a buffer circuit, and their related features conceded to be absent from *Edwards*. However, *Yamazaki*

offers no disclosure or suggestion of the above-described features that are also absent from *Edwards*.

Specifically, "*wherein the buffer circuit includes an analog buffer circuit and a precharge circuit,*" and "*executing a precharge processing for the precharge period by disconnecting the precharge circuit for the precharge period from the analog buffer circuit*" are not disclosed, taught or suggested by *Yamazaki*.

In addition, since *Edwards* does not teach or suggest Applicant's claimed features and since *Yamazaki* offers no disclosure or suggestion regarding Applicant's claimed features, an artisan would not be inclined to combine *Yamazaki* with *Edwards*.

Accordingly, since even a combination of *Edwards* and *Yamazaki* would still fail to yield features of Applicant's claimed invention, a *prima facie* case of obviousness for independent claim 1 has not been presented.

For reasons similar to those provided for claim 1, independent claims 3 and 5 are neither disclosed, taught, or suggested by *Edwards* and *Yamazaki*. The dependent claims are also distinct for their incorporation of the features respectively recited in the independent claims as well as for their own, separately recited patentably distinct features.

Specifically, regarding claim 2, repeating the period when the voltage between terminals of the capacitor for sampling is set in not disclosed in *Edwards*.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 1-6 under 35 U.S.C. § 103(a) as being unpatentable over *Edwards* and *Yamazaki*.

In view of the above amendment, applicant believes the pending application is in condition for allowance. If any further issues remain, the Examiner is invited to telephone the undersigned to resolve them.

Please treat any concurrent or future reply, requiring a petition for an extension of time under 37 C.F.R. §1.136, as incorporating a petition for extension of time for the appropriate length of time.

This response is believed to be a complete response to the Office Action. However, Applicant reserves the right to set forth further arguments supporting the patentability of their claims, including the separate patentability of the dependent claims not explicitly addressed herein, in future papers. Further, for any instances in which the Examiner took Official Notice in the Office Action, Applicant expressly does not acquiesce to the taking of Official Notice, and respectfully requests that the Examiner provide an affidavit to support the Official Notice taken in the next Office Action, as required by 37 CFR 1.104(d)(2) and MPEP § 2144.03.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 18-0013, under Order No. SON-3056 from which the undersigned is authorized to draw.

Dated: April 15, 2011

Respectfully submitted,

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